Amendments to the Specification:

Please amend the paragraph beginning at page 6, line 26 as follows:

FIGS. ~~4 and 4A~~ 4A and 4B illustrate alternative embodiments of a memory architecture in which main microcode ROM and main microcode RAM share a common memory address area, along with a "select" RAM bit used to control the selection of main microcode ROM or main microcode RAM for execution. In FIG. 4A, all microcode ROM is associated with an area of microcode RAM. In FIG. 4B, all microcode ROM shares a common address with microcode RAM, but additional address areas for microcode RAM are allocated to accept new microcode.

Please amend the paragraph beginning at page 7, line 32 as follows:

FIG. 9 is a block diagram showing the functional implementation of the memory architecture illustrated in ~~FIG. 4~~ FIGS. 4A and 4B.

Please amend the paragraph beginning at page 18, line 10 as follows:

Figures ~~4 and 4A illustrates~~ 4A and 4B illustrate an architecture in which ROM (1101 or 1101a), RAM (1103) and a RAM select bit share a common address. The select bit is used to

determine whether the associated RAM or ROM instructions are to be executed.

Please amend the paragraph beginning at page 18, line 30 as follows:

Figure 9 illustrates a system for implementing the memory architecture shown in ~~Figure 4~~ Figures 4A and 4B. To execute a microcode instruction, the program counter (1601) simultaneously addresses main ROM (1101), main RAM (1103), and a RAM select bit (1102). The ROM (1101) microcode and RAM (1103) microcode held in the selected address are input to a multiplexer (1602). The RAM select bit (1102) is used by the multiplexer to control the selection of ROM microcode or RAM microcode as the output of the multiplexer. Depending upon the status of the select bit, the multiplexer selects either the ROM microcode or the RAM microcode for output and further processing. The microcode selected for output from the multiplexer is then executed and the program counter incremented or branched as necessary to initiate the next microcode instruction routine.